REMARKS

Claims 1 - 17 remain active in this application. Claim 11 has been amended to improve clarity. Support for the amendments of the claims is found throughout the application, particularly in Figures 2 - 4 and the description thereof on pages 8 - 11 of the specification as originally filed. No new matter has been introduced into the application.

The indication of the allowability of the subject matter of claims 5, 9 and 16 is noted with appreciation. The indication of acceptance of the formal drawings filed on December 22, 2004, and consideration of the documents cited in the Information Disclosure Statement are also noted with appreciation.

Claims 1 - 4, 6 - 8 and 10 have been rejected under 35 U.S.C. §103 as being unpatentable over Bhat in view of Yamada et al. and claims 11 - 15 and 17 have been rejected under 35 U.S.C. §102 as being anticipated by Sone et al. Both of these grounds of rejection are respectfully traversed.

The invention is directed to a technique of suppressing codes which are not needed by a processor when operating in a particular mode or when various peripheral devices may or may not be present. The invention thus can avoid decoding and storage of operations of an application program which will not be needed to improve execution time (e.g. by reducing cache misses or the like since more operations which are likely to be used can be stored locally to the processor) and, more importantly, can save time and power during initialization so that the processor can be re-started, if necessary, in substantially real time.

This meritorious function is achieved without alteration of the application program by inserting execution bits into operation codes of the sequence of

operations which form the application program in accordance with the mode of operation or peripheral devices, if any, which are connected to the processor when the processor is initialized. Then, as the operation codes are decoded and stored, the state of the execution bit of a current operation being decoded is used to control whether decoding will be continued, in sequence, through the sequence of operation codes or whether one or more subsequent operation codes are to be skipped. This type of control also allows the skipping of operations to be performed in a very simple manner which may be rapidly executed, for example, by simply incrementing the instruction counter. Thus, in effect, a conditional branch is made available for each operation code and may result, when an unused/unusable operation or group of operations is skipped, in avoiding many branching operations which are slow to execute in the decoding and storage process. It is respectfully submitted that none of the prior art applied by the Examiner has anything to do with such a function, problem or its solution or lead to any expectation of success in producing the meritorious effects of the invention by the simple expedient provided by the invention.

Specifically, Bhat is directed to a wireless cellular communication system capable of either voice communications or paging. Voice messaging is directed through "components" of the system "such as...radio cluster servers" (see column 4, lines 15 - 20; the passage of column 5 cited by the Examiner indicates that software is preferred to hardware, which can be alternatively used, for the network interface module and communication module but does not mention the radio cluster servers) which are bypassed if the message is a paging message and the processing provided by those "components" provide no functionality in a paging message while such "components" may have limited

message handling capacity. Thus, Bhat is directed to bypassing of *hardware* during *normal operation* of the communication system *and while the radio cluster servers remain in use* for voice messages and has nothing to do with bypassing of *(software) operation codes* during *initialization of the processor when the operation codes are decoded and stored* in order to reduce program storage requirements and save decoding time and power and storage space during initialization while improving execution speed when the program is later executed. It is also respectfully submitted that the equating of software *modules* with operation codes in the statement of the rejection by the Examiner is incorrect and, at best, an exercise in impermissible hindsight. Therefore, Bhat does not answer *any* of the method steps of claims 1 - 10 or *any* of the elements of claims 11 - 17 and is thus seen to be essentially irrelevant to the claimed invention.

Yamada et al. is directed to reducing the number of bits in a condition execution field of a condition execution instruction to determine whether or not that instruction will be executed when reached for execution. It is clear, even from the Abstract of Yamada et al., that the execution code field controls *execution* of the *decoded* instruction *in which the execution field is present* at the time the instruction is reached *during execution of the program* and has nothing to do with *bypassing* decoding and/or storage of *other* operation *codes* during *initialization of the processor*. Therefore, Yamada et al. does not answer the recitations of any claim in the application and certainly does not mitigate the numerous deficiencies of Bhat to do so. Nor, it is respectfully submitted, is Yamada et al. properly combinable with Bhat since, contrary to the teachings of Bhat, Yamada et al. suggests suppression of the *function* of operation codes rather than bypassing them. That is, if the radio

cluster servers of Bhat were, in fact, software, as the Examiner erroneously asserts, modification in accordance with Yamada et al. would lead to passing paging messages through the radio cluster servers while suppressing the functions thereof rather than bypassing the radio cluster servers altogether.

Accordingly, it is respectfully submitted that the rejection based on the combination of Bhat and Yamada et al. is clearly erroneous for a number of reasons discussed above and the Examiner has failed to make a *prima facie* demonstration of obviousness of any claim in the application while effectively ignoring explicit recitations of the claims and improperly construing the references relied upon through hindsight and largely contrary to the actual teachings thereof. Accordingly, reconsideration and withdrawal of the rejection based on Bhat and Yamada et al is respectfully requested.

In regard to Sone et al., it is clear that the statement of the rejection relies on the breadth of the Examiner's construction of claim 11 as being readable on any branching operation. While the Examiner's broad construction of "execution bit" is correct and appreciated, the remainder of the statement of the rejection is incorrect and clearly is grounded in the Examiner's confusion between "program flow" during "execution or processing", asserted to be taught by Sone et al., and suppression of *instructions* (e.g. code in a form which can be processed/decoded and/or stored) in accordance with the invention. Note, for example, the last sentence of the Abstract of Sone et al. where it is stated that "*operations* for *executing* a new command" are "*suspended*" upon detection of a *branch condition* as opposed to *bypassing* an *instruction* based on an execution bit (in another instruction) in accordance with the invention.

That is, the Examiner has not demonstrated how Sone et al. answers the recitations of "*each* said

instruction including an execution bit" in combination with "means for *bypassing an instruction* of said sequence based on a particular state of an execution bit in a *current* instruction" (emphasis added) as recited in claim 11 as originally filed which clearly and unambiguously refers to the instruction itself (e.g. processing the instruction as distinguished from executing or performing the instruction) and not its function when executed and distinguishes the instruction which is to be bypassed from the instruction containing the execution bit which causes the instruction to be bypassed and such that the bypassing operation can be performed with great flexibility as to the instructions to be bypassed and with a granularity of a single and arbitrary instruction.

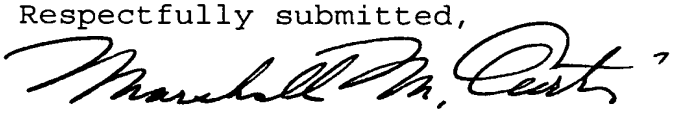
Therefore, the Examiner has failed to make a *prima facie* demonstration of anticipation by Sone et al. of any claim in the application as originally filed. Nevertheless, claim 11 has been amended to clarify and emphasize the distinction at the point of the Examiner's apparent confusion and it is respectfully submitted that Sone et al. clearly does not anticipate amended claim 11 or claims depending therefrom and does not contain teachings or suggestions which would support a conclusion of obviousness in regard to any claim in the application. Accordingly, reconsideration and withdrawal of the rejection based on Sone et al. is respectfully requested.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that

this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Deposit Account No. 09/0456 of International Business Machines Corporation (Burlington).

Respectfully submitted,



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